CLAIMS:

We claim:

1. A method of forming a microelectronic structure on a semiconductor material having a silicon surface layer on a substrate, comprising the steps of:
    a. implanting first dopant ions onto the surface layer;
    b. subjecting the semiconductor material to a first annealing process; and
    c. subjecting the semiconductor material to a second annealing process.

2. The method of claim 1, comprising the step of implanting second dopant ions of a second conductivity type opposite in polarity to the first conductivity type onto the surface layer, and wherein the step of implanting second dopant ions occurs:
    a. at an acceleration energy from 50 eV to 5000 eV; and
    b. with a dosage from $1\times10^{13}/cm^2$ to $1\times10^{16}/cm^2$.

3. The method of claim 1, wherein the step of implanting first dopant ions comprises at least one high energy implantation step greater than 200keV, and at least one low energy implantation step less than 5keV.

4. The method of claim 3, wherein the high-energy ion implantation step is carried out:
    a. at an energy level of about 200 keV to about 2000 keV; and
    b. with a dosage from $1\times10^{13}/cm^2$ to $1\times10^{17}/cm^2$.

5. The method of claim 1, wherein the first annealing process comprises:
   a. heating the semiconductor material from about 800°C to about 1200°C with a ramp-up rate of about 50°C per second to about 1000°C per second; and
   b. after reaching a first desired temperature, holding the temperature for a time period from about 1 millisecond to about 1000 seconds.

6. The method of claim 1, wherein the first annealing process includes a cooling process that comprises cooling the semiconductor material at a ramp-down rate from about 50°C per second to about 500°C per second.

7. The method of claim 1, wherein the second annealing process comprises heating the semiconductor material at a temperature from about 400°C to about 650°C, for a time period from about 1 second to about 10 hours.

8. The method of claim 1, wherein the second annealing process comprises heating the semiconductor material with such temperature, amount of time, and heating and cooling rates so that minimal dopant diffusion occurs.

9. The method of claim 1, wherein at least a part of the first and second annealing processes occur in one selected from the group consisting of: a vacuum, nitrogen gas, and inert gas.

10. The method of claim 2, wherein the second dopant ions are selected from the group consisting of boron, arsenic, phosporus, and antimony.

11. The method of claim 2 wherein the second dopant ions have a concentration of about $1\text{x}10^{16}$ ions/cm^3 to about $1\text{x}10^{21}$ ions/cm^3.

12. The method of claim 1 wherein the second annealing process occurs any time after the first annealing process.

13. A method of forming a microelectronic structure on a semiconductor material by molecular beam epitaxy growth, comprising the steps of:

a. exposing, in a vacuum chamber, a single crystal semiconductor body to a flux of one or more atomic or molecular species, with the body maintained at a temperature greater than about 100°C and less than about 800°C;

b. depositing a single crystal epitaxial layer with doped atoms that are electrically active; and

c. subjecting the semiconductor material to a post-growth annealing process.

14. The method of claim 13, wherein the annealing process occurs *in situ* in one selected from the group consisting of: a vacuum, nitrogen gas, and inert gas.

15. The method of claim 13, wherein the annealing process comprises heating the semiconductor material with such temperature, amount of time, and heating and cooling rates so that minimal dopant diffusion occurs.